

In re Patent Application of:

**MEARS ET AL.**

Serial No. 10/647,069

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In the Specification:

Please amend paragraph [0032] beginning on page 10 as follows:

The illustrated MOSFET 20 includes a substrate 21, source/drain regions 22, 23, source/drain extensions 26, 27, and a channel region therebetween provided by the superlattice 25. Source/drain silicide layers 30, 31 and source/drain contacts 32, 33 overlie the source/drain regions as will be appreciated by those skilled in the art. Regions indicated by dashed lines 34, 35 are optional vestigial portions formed originally with the superlattice, but thereafter heavily doped. In other embodiments, these vestigial superlattice regions 34, 35 may not be present as will also be appreciated by those skilled in the art. A gate ~~35~~ 38 illustratively includes a gate insulating layer 37 adjacent the channel provided by the superlattice 25, and a gate electrode layer 36 on the gate insulating layer. Sidewall spacers 40, 41 are also provided in the illustrated MOSFET 20.

Please amend paragraph [0037] beginning on page 10 as follows:

As will be appreciated by those skilled in the art, the source/drain regions 22, 23 and gate ~~35~~ 38 of the MOSFET 20 may be considered as regions for causing the transport of charge carriers through the superlattice in a parallel direction

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relative to the layers of the stacked groups **45a-45n**. Other such regions are also contemplated by the present invention.

Please amend paragraph [0059] beginning on page 10 as follows:

FIG. 6G shows the spacer **428** formation and the source and drain implants. An SiO<sub>2</sub> mask is deposited and etched back. N-type and p-type ion implantation is used to form the source and drain regions **430**, **432**, **434**, and **436**. Then the structure is annealed and cleaned. FIG. 6H depicts the self-aligned silicides **438** formation, also known as salicidation. The salicidation process includes metal deposition (e.g. Ti), nitrogen annealing, metal etching, and a second annealing. This, of course, is just one example of a process and device in which the present invention may be used, and those of skill in the art will understand its application and use in many other processes and devices. In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer. ~~In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer.~~